ABSTRACT OF THE DISCLOSURE:

A memory system of a high-speed operation can be realized by reducing an influence of reflection signals etc. caused by branching and impedance mismatching in various wirings between a memory controller and a memory module, and an influence due to transmission delays of data, command/address, and clocks in the memory module. To this end, a memory system comprises a memory controller and a memory module mounted with DRAMs. A buffer is mounted on the memory module. The buffer and the memory controller are connected to each other via data wiring, command/address wiring, and clock wiring. The DRAMs and the buffer on the memory module are connected to each other via internal data wiring, internal command/address wiring, and internal cock wiring. The data wiring, the command/address wiring, and the clock wiring may be connected to buffers of other memory modules in cascade. Between the DRAMs and the buffer on the memory module, high-speed data transmission is implemented using data phase signals synchronous with clocks.